

LOW-CAPACITANCE 2-CHANNEL ± 15 -kV ESD-PROTECTION ARRAY FOR HIGH-SPEED DATA INTERFACES

FEATURES

- ESD Protection Exceeds
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC 61000-4-2 Contact Discharge
 - ± 15 -kV IEC 61000-4-2 Air-Gap Discharge
- Low 1.5-pF Input Capacitance
- Low 1-nA (Max) Leakage Current
- Low 1-nA Supply Current
- 0.9-V to 5.5-V Supply-Voltage Range
- Two-Channel Device
- Space-Saving DRL, DRY, and QFN Package Options
- Alternate 3-, 4-, 6-Channel Options Available: TPD3E001, TPD4E001, and TPD6E001

APPLICATIONS

- USB 2.0
- Ethernet
- FireWire™
- Video
- Cell Phones
- SVGA Video Connections
- Glucose Meters

DESCRIPTION/ORDERING INFORMATION

The TPD2E001 is a low-capacitance ± 15 -kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The TPD2E001 protects against ESD pulses up to ± 15 -kV Human-Body Model (HBM), ± 8 -kV Contact Discharge, and ± 15 -kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a 1.5-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

The TPD2E001 is a two-channel device intended for USB and USB 2.0 applications.

The TPD2E001 is available in DRL, DRY, and thin QFN packages and is specified for -40°C to 85°C operation.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) – YFP (Pb-free)	Tape and reel	TPD2E001YFPR	PREVIEW
	SOP – DZD	Tape and reel	TPD2E001DZDR	NFGO
	1.6 × 1.6 SOP (SOT-533) – DRL	Reel of 4000	TPD2E001DRLR	2AR
	1.45 × 1 SON – DRY	Reel of 5000	TPD2E001DRYR	2A
	3 × 3 QFN – DRS	Reel of 1000	TPD2E001DRSR	ZWK

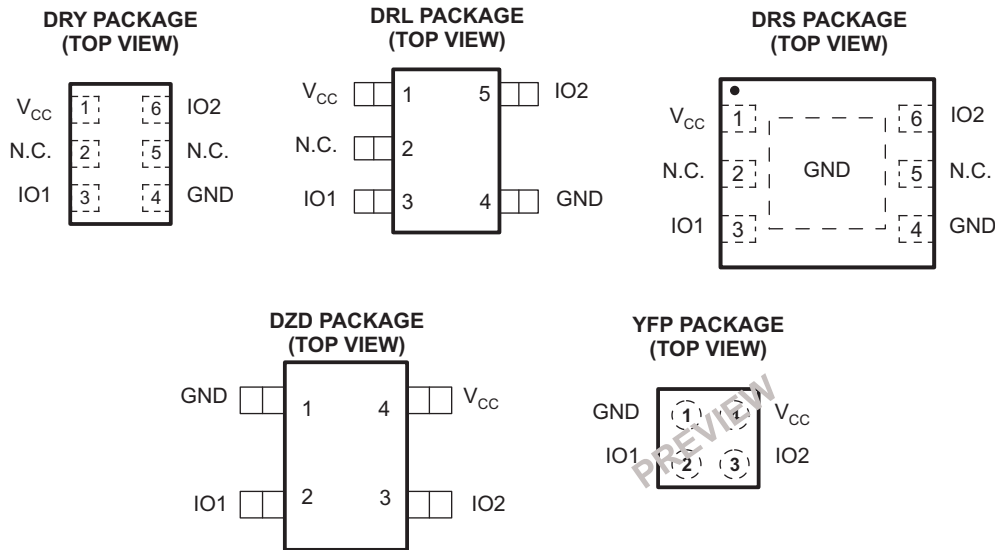
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



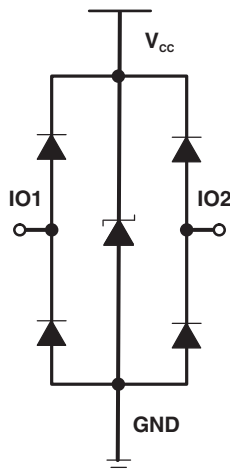
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N.C. – Not internally connected

LOGIC BLOCK DIAGRAM



PIN DESCRIPTION

DRS NO.	DRL NO.	DRY NO.	NAME	FUNCTION
3, 6	3, 5	3, 6	IO _x	ESD-protected channel
4	4	4	GND	Ground
1	1	1	V _{CC}	Power-supply input. Bypass V _{CC} to GND with a 0.1-μF ceramic capacitor.
2, 5	2	2, 5	N.C.	No connection. Not internally connected.
EP			EP	Exposed pad. Connect to GND.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		-0.3	7	V
V_{IO}		-0.3	$V_{CC} + 0.3$	V
T_{stg}	Storage temperature range	-65	150	°C
T_J	Junction temperature		150	°C
Bump temperature (soldering)	Infrared (15 s)		220	°C
	Vapor phase (60 s)		215	
Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	$I_F = 10\text{ mA}$		0.65		0.95	V
V_{BR}	Breakdown Voltage	$I_{BR} = 10\text{ mA}$		11			V
V_C	Channel clamp voltage ⁽²⁾	$T_A = 25^\circ\text{C}$, $\pm 15\text{-kV HBM}$, $I_F = 10\text{ A}$	Positive transients			$V_{CC} + 25$	V
			Negative transients			-25	
		$T_A = 25^\circ\text{C}$, $\pm 8\text{-kV Contact Discharge}$ (IEC 61000-4-2), $I_F = 24\text{ A}$	Positive transients			$V_{CC} + 60$	
			Negative transients			-60	
		$T_A = 25^\circ\text{C}$, $\pm 15\text{-kV Air-Gap Discharge}$ (IEC 61000-4-2), $I_F = 45\text{ A}$	Positive transients			$V_{CC} + 100$	
			Negative transients			-100	
$I_{i/o}$	Channel leakage current	$V_{i/o} = \text{GND to } V_{CC}$				± 1	nA
$C_{i/o}$	Channel input capacitance	$V_{CC} = 5\text{ V}$, Bias of $V_{CC}/2$			1.5		pF

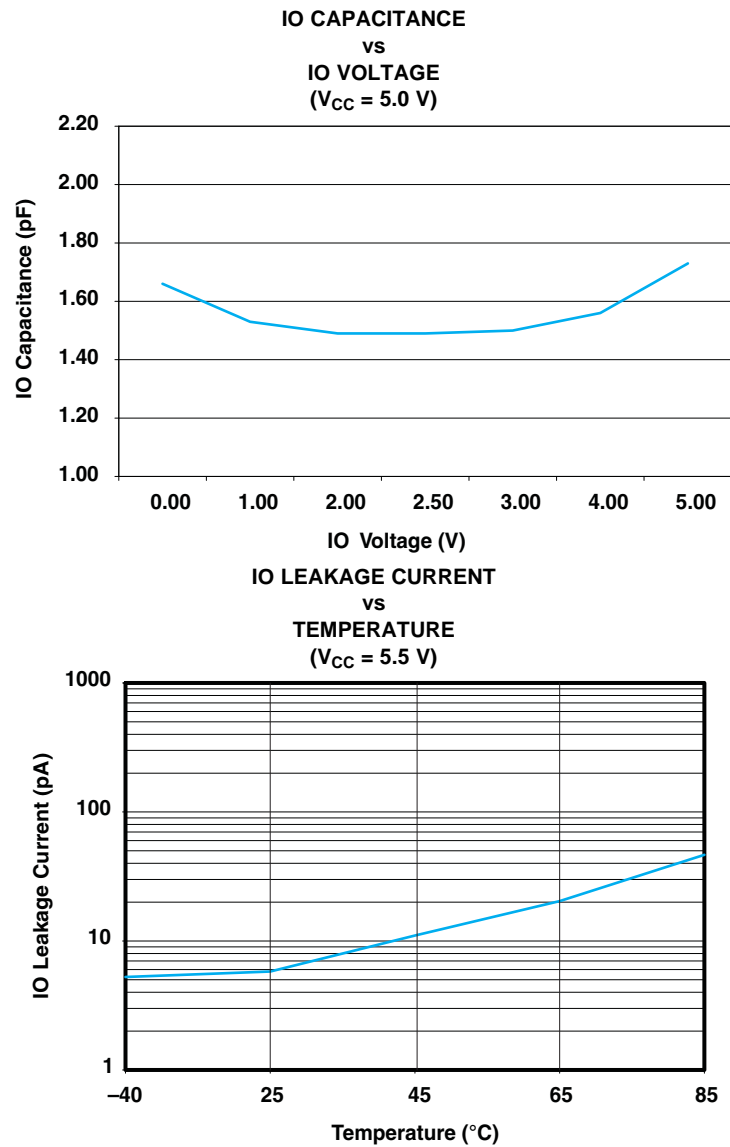
(1) Typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$

(2) Channel clamp voltage is not production tested.

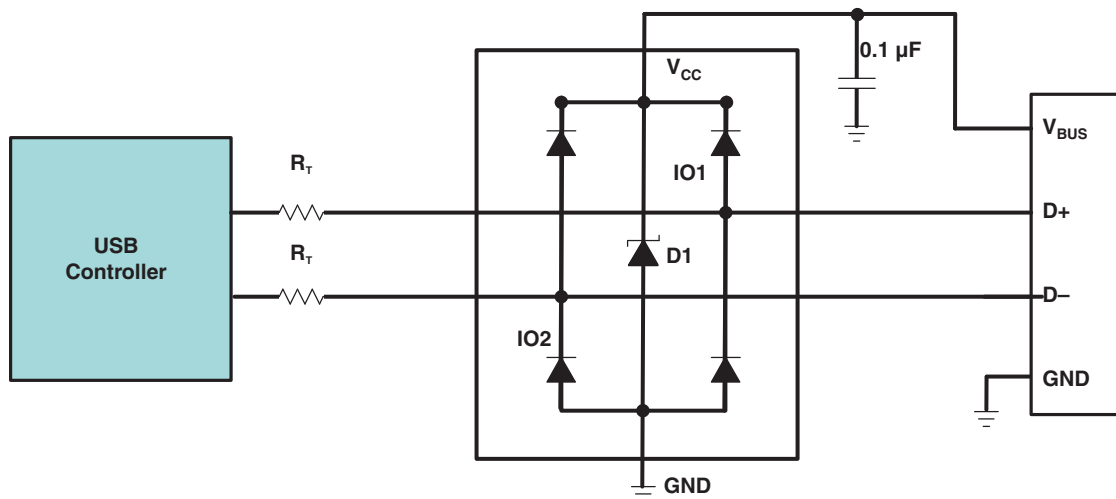
ESD PROTECTION

PARAMETER	TYP	UNIT
HBM	± 15	kV
IEC 61000-4-2 Contact Discharge	± 8	kV
IEC 61000-4-2 Air-Gap Discharge	± 15	kV

TYPICAL OPERATING CHARACTERISTICS



APPLICATION INFORMATION



Detailed Description

When placed near the connector, the TPD2E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD2E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD2E001 solution close to the connector. This allows the TPD2E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1- μF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Make sure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD2E001 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating.
5. The V_{CC} pin can be connected in two different ways:
 - a. If the V_{CC} pin is connected to the system power supply, the TPD2E001 works as a transient suppressor for any signal swing above $V_{CC} + V_F$. A 0.1- μF capacitor on the device V_{CC} pin is recommended for ESD bypass.
 - b. If the V_{CC} pin is not connected to the system power supply, the TPD2E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1- μF capacitor is still recommended at the V_{CC} pin for ESD bypass.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPD2E001DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD2E001DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD2E001DRSR	ACTIVE	SON	DRS	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPD2E001DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD2E001DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD2E001DZDR	ACTIVE	SOP	DZD	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E001DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
TPD2E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD2E001DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPD2E001DZDR	SOP	DZD	4	3000	179.0	8.4	3.15	2.6	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

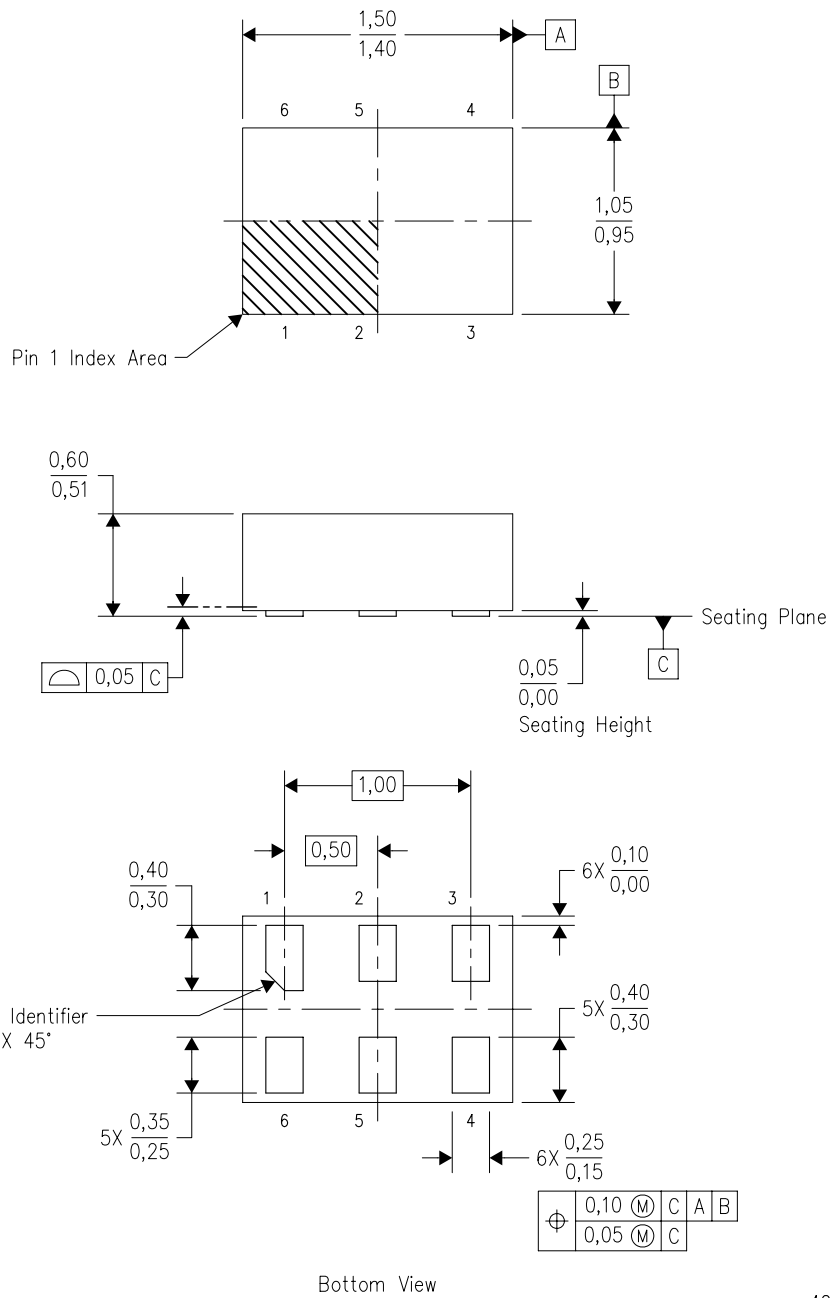
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E001DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
TPD2E001DRSR	SON	DRS	6	1000	346.0	346.0	29.0
TPD2E001DRYR	SON	DRY	6	5000	220.0	205.0	50.0
TPD2E001DZDR	SOP	DZD	4	3000	195.0	200.0	45.0



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DRY (R-PDSO-N6)

PLASTIC SMALL OUTLINE



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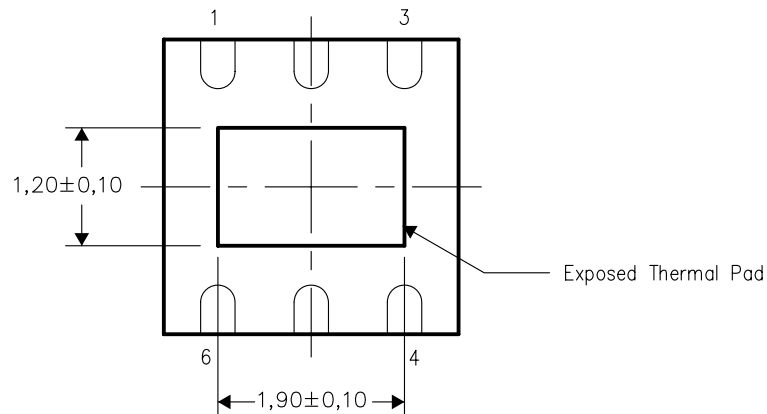
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.
 - This package complies to JEDEC MO-287 variation UFAD.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

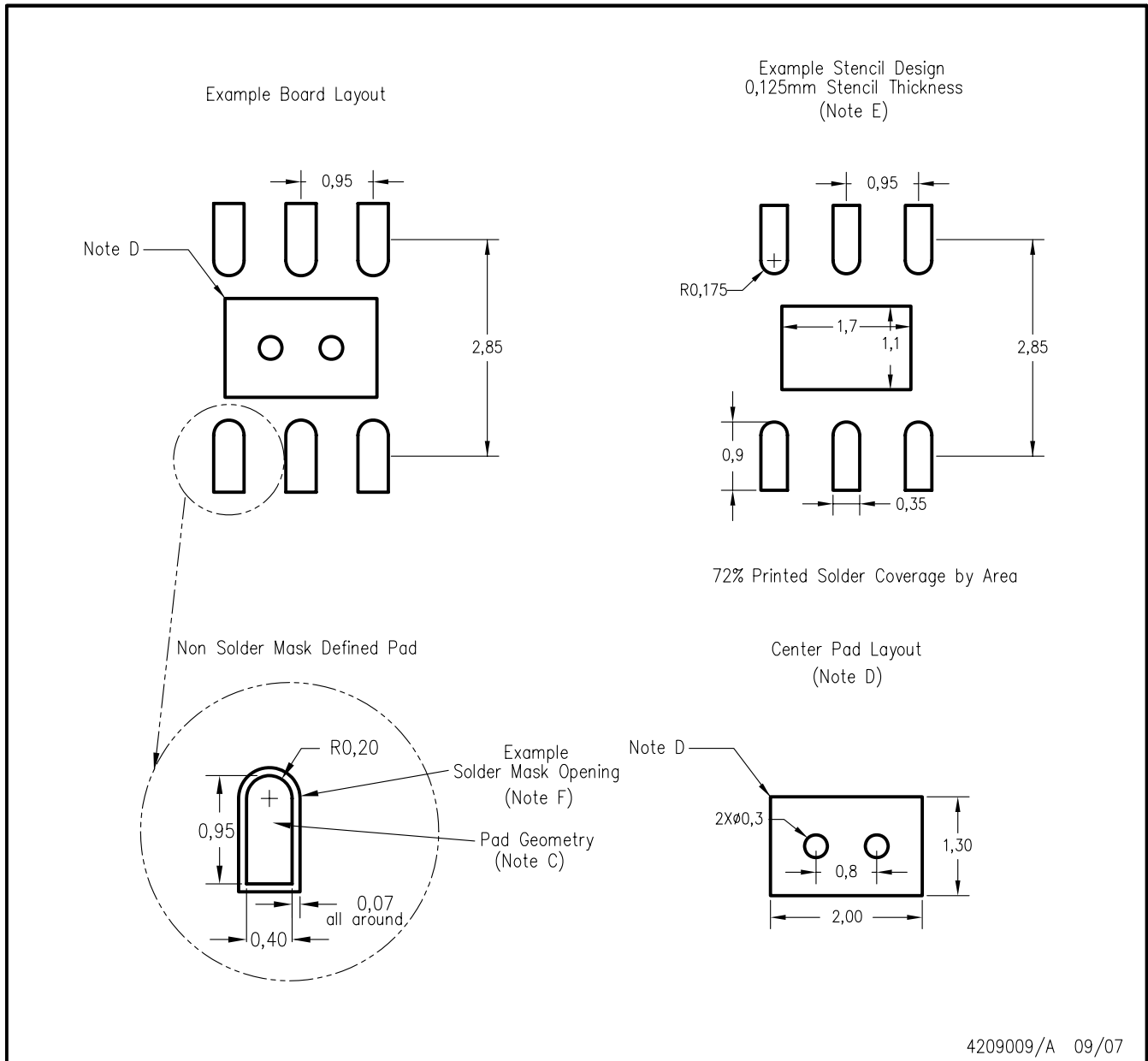


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

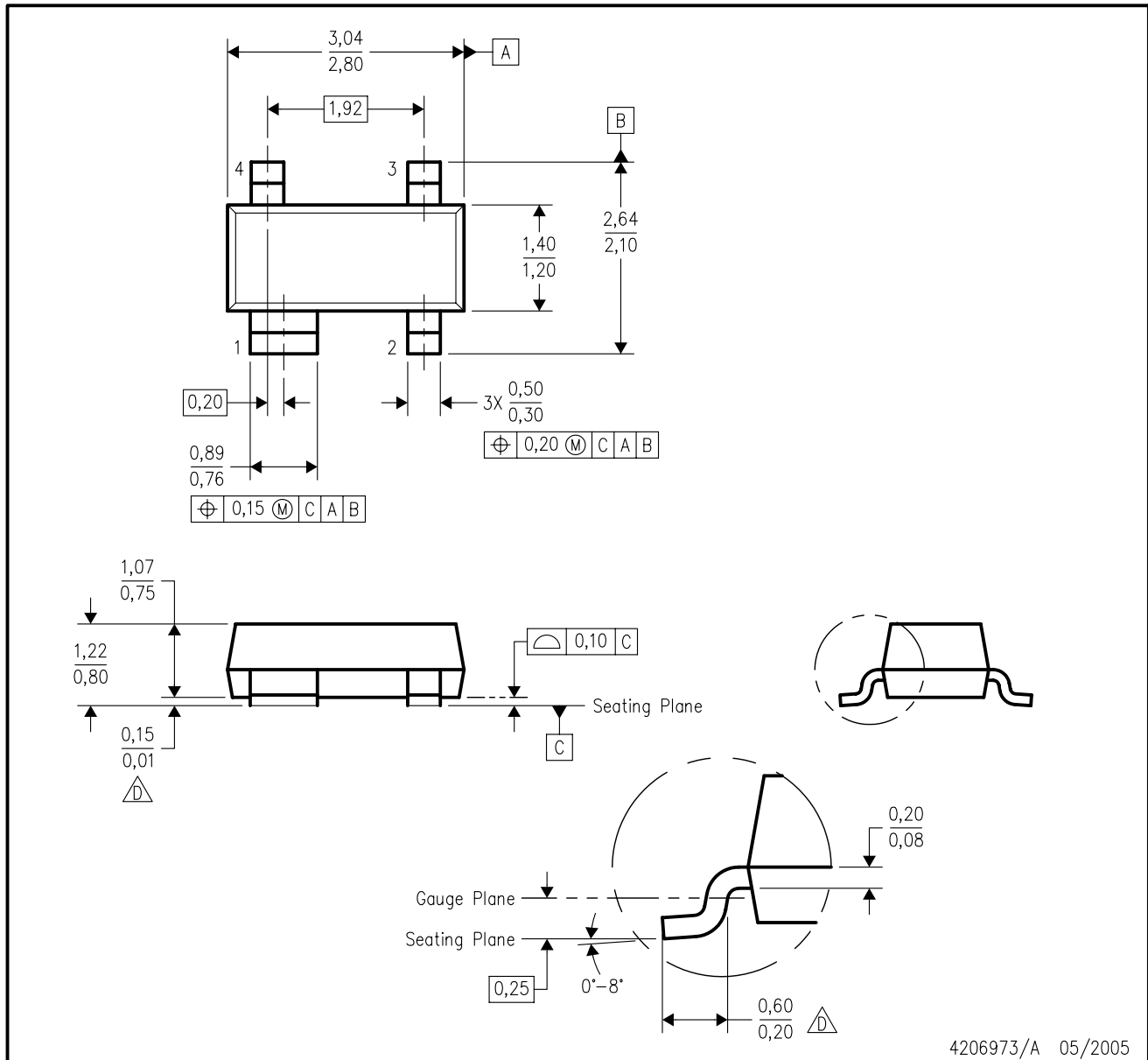
DRS (S-PDSO-N6)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

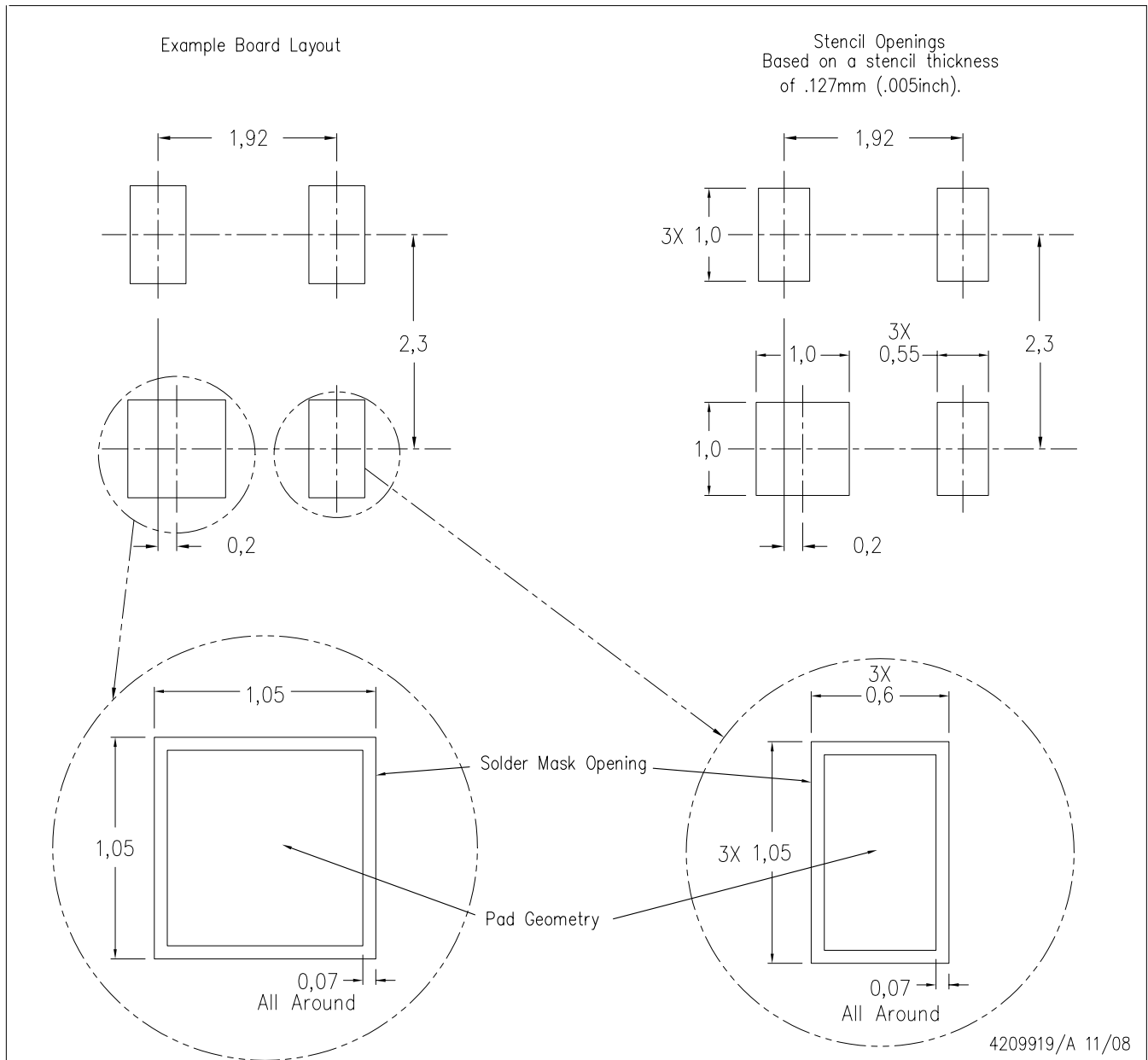
DZD (R-PDSO-G4)

PLASTIC SMALL-OUTLINE



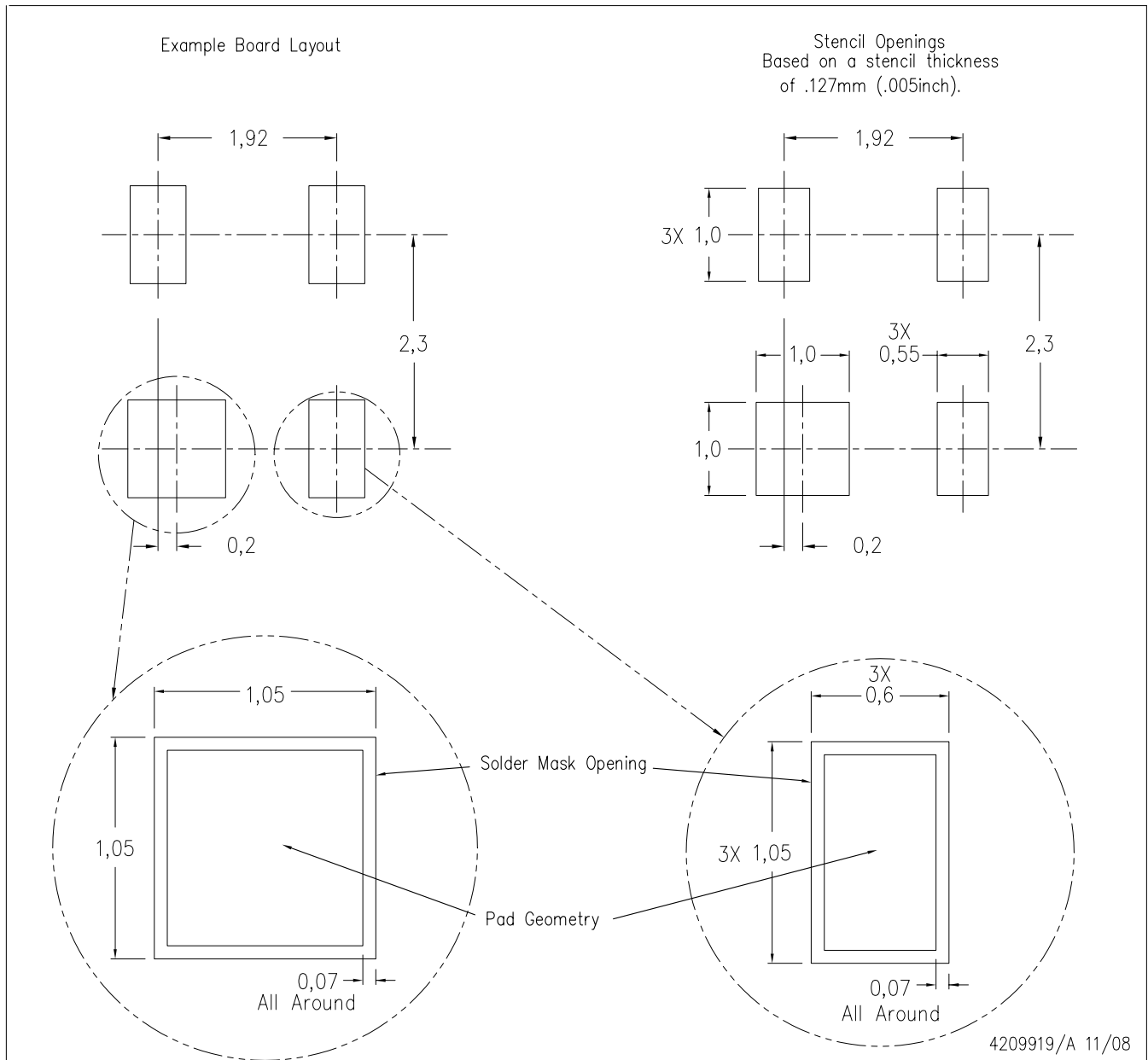
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.25 per side.
 - ⚠ Falls within JEDEC TO-253 variation AA, except minimum foot length and minimum seating height.

DZD (R-PDSO-G4)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

DZD (R-PDSO-G4)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

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